PTO/SB/08B (Substitute for form 1449/PTO)	Attorney Docket No.:	*004-8907*
	Application No.:	*10/651,113*
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor:	*Aveek Sarkar et al.*
	Filing Date:	*August 28, 2003*
	Group Art Unit:	*2858*
	Examiner Name:	*(Unassigned)*
Sheet 1 of 1	Date Submitted:	*September 19, 2005*
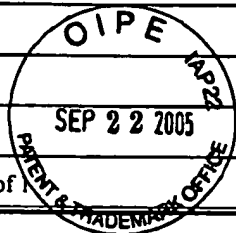
NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
PS		"Synopsys and Texas Instruments", product description , 6 pages, Synopsys, Inc., copyright 1999.	
PS		Yalcin, et al. "An Advanced Timing Characterization Method Using Mode Dependency", Proceedings of the 38th Conference on Design Automation (DAC'01), pp. 657-660, June 18-22, 2001.	
PS		Agah, Hamid, "Physical Synthesis", Application Note: FPGAs, from XILINX®, XAPP140, (v1.0), 3 pages, Xilinx, Inc., February 26, 2001.	
PS		"PathMill: Transistor-Level Static Timing Analysis ", 3 pages, Sysnopsys Products & Solutions, Synopsys, Inc., downloaded from http://www.synopsys.com/products, on or about May 2003.	
PS		Bray, Jeffrey, Sr., "Verifying timing of external IP key to SoC success", EE Times, May 28, 2002, 3 pages, downloaded from http://www.eetimes.com, May 14, 2003.	
PS		"Transistor and gate level full chip timing analysis and automatic block characterization", product description from Dyna, 3 pages, downloaded from www.circuitsemantics.com, May 14, 2003.	
PS		"PrimeTime Synopsys Static Timing Solution", 13 pages, 07/29/99, Revision 1.9, Sysnopsys Products & Solutions, Synopsys, Inc., downloaded from http://www.synopsys.com/products on June 5, 2003.	

Examiner Signature		Date Considered	7/10/07

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[1]Applicant's unique citation designation number (optional).

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